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SIDDHARTH INSITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester Supplementary Examinations November-2020
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 hours   Max. Marks: 60

PART-A
(Answer all the Questions **5 x 2 = 10** Marks)

1	a	State DeMorgan's theorems.	2M
	b	Simplify the given Boolean function using K-Map $F(X,Y,Z) = \sum(1,2,3,6,7)$.	2M
	c	What is master-slave flip-flop?	2M
	d	Compare PAL, PLA & PROM.	2M
	e	Write a VHDL Program for Half Adder in Dataflow Model.	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Perform the 10's complement Subtraction for the given numbers. i) 3456 – 245 ii) 1631-745	6M
	b	Convert the following to binary and then to gray code. i) $(1111)_{16}$ ii) $(BC54)_{16}$	4M

OR

3	a	Obtain the truth table of the following Boolean function and express the function as sum of minterms and product of maxterms $F = (A+B) (B+C)$.	6M
	b	Simplify the following Boolean functions to minimum number of literals. i) F=xy+x'z+yz ii) F=x'y'z+x'yz+xy' iii) F= (x+y)'(x'+y') iv) F=xy+xy'+x'y	4M

UNIT-II

4	a	Minimize the following Boolean function using K-map i) F (A, B, C, D) = Σm(1,4,5,6,12,13,14,15). ii) F (A, B, C, D, E) =∑ (0,1,4,5,16,17,21,25,29).	5M
	b	Explain the procedure for designing a combinational circuit.	5M

OR

5	a	Design & implement a Full Adder.	5M
	b	Design & Implement an 8:1 Multiplexer.	5M

UNIT-III

6	a	Implement D-FF using JK FF with its truth table.	5M
	b	Give the characteristic table, Truth table, characteristic equation and excitation table for D FlipFlop.	5M

OR

7	a	Design and implement a Mod-10 Synchronous Up counter using T-FFs.	5M
	b	Draw and explain a 4-bit Serial in Serial out (SISO) Shift Register.	5M

<div align="center">**UNIT-IV**</div>

8	**a**	What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions.	**6M**
	b	Explain the following specifications (i) Fan out (ii) Noise margin	**4M**

<div align="center">**OR**</div>

9	**a**	Implement the following Boolean function using PAL. (i) $F1\ (w,x,y,z) = \Sigma m(0,1,2,3,7,9,11)$ (ii) $F2\ (w,x,y,z) = \Sigma m(0,1,2,3,10,12,14)$	**6M**
	b	Implement NAND and NOR operations using CMOS logic.	**4M**

<div align="center">**UNIT-V**</div>

10	**a**	Explain various data objects in VHDL. Give necessary examples.	**5M**
	b	Explain the structure of a VHDL program.	**5M**

<div align="center">**OR**</div>

11	**a**	Write a VHDL program for Full Subtractor.	**5M**
	b	Write a VHDL program for a D and T FF.	**5M**

<div align="center">***END***</div>